

LZ23242J

1/3 type B/W CCD Area Sensor for CCIR

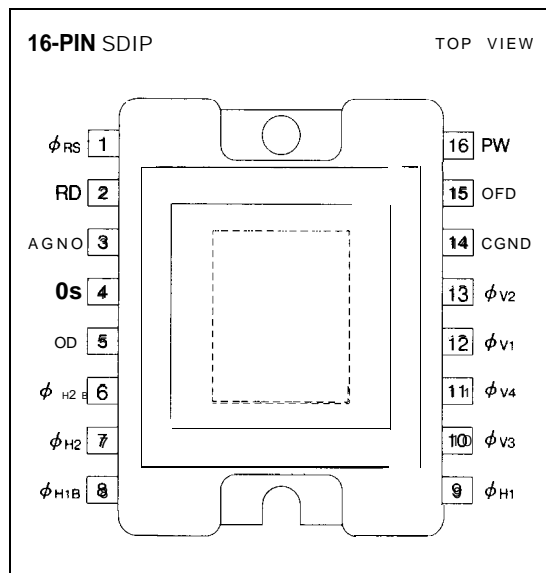
DESCRIPTION

LZ23242J is a 1/3-type (6.0 mm) solid state image sensor that consists of PN photo-diodes and CCDs (charge-coupled devices). Having approximately 320000 pixels (horizontal 542 x vertical 562), the sensor provides a high resolution stable B/W normal or mirror image.

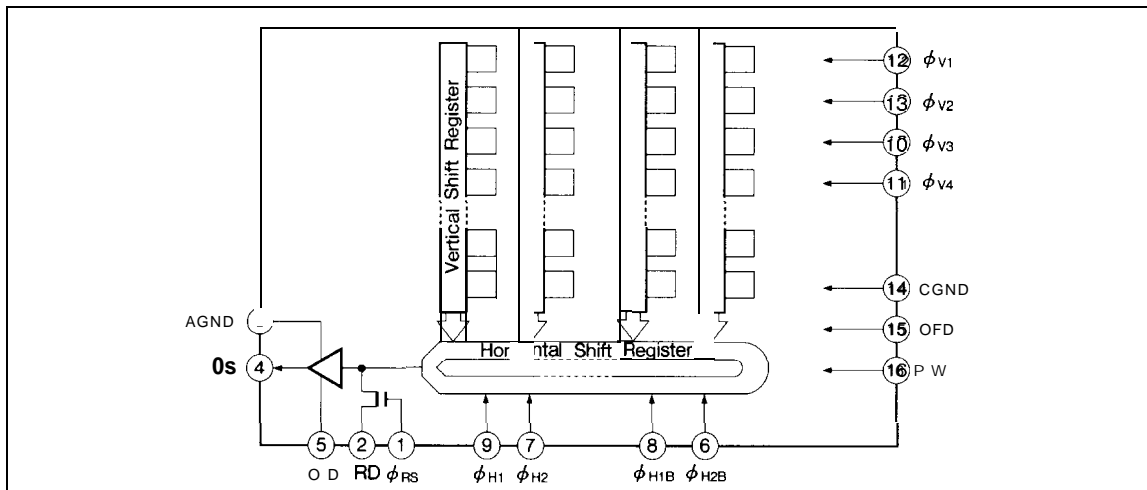
FEATURES

- Number of pixels : 512 (H) x 582 (V)
Pixel pitch : 9.6 μm (H) x 6.3 μm (V)
Number of optical black pixels
: Horizontal; front 2 and rear 28
- Low fixed pattern noise and lag
- No sticking and no image distortion
- Blooming suppression structure
- Built-in output amplifier
- Variable electronic shutter (1/50 to 1/10000 s)
- Compatible with CCIR standard
- Normal or mirror image output available from common output terminal
- Package : 16-pin SDIP [CERDIP] (WDIP016-N-0500B)

PIN CONNECTIONS



BLOCK DIAGRAM



PIN DESCRIPTION

| SYMBOL | PIN NAME | NOTE |
|--|--------------------------------------|------|
| RD | Reset transistor drain | |
| OD | Output transistor drain | |
| OS | Video output | |
| ϕ_{RS} | Reset transistor gate clock | |
| $\phi_{V1}, \phi_{V2}, \phi_{V3}, \phi_{V4}$ | Vertical shift register gate clock | |
| $\phi_{H1}, \phi_{H2}, \phi_{H1B}, \phi_{H2B}$ | Horizontal shift register gate clock | 1 |
| OFD | Overflow drain | |
| PW | P type well | |
| AGND | Analog part ground | |
| CGND | Clock part ground | |

NOTE :

- 1 Normal image output mode : $\phi_{H1} = \phi_{H1B}, \phi_{H2} = \phi_{H2B}$
 Mirror image output mode : $\phi_{H1} = \phi_{H2B}, \phi_{H2} = \phi_{H1B}$

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

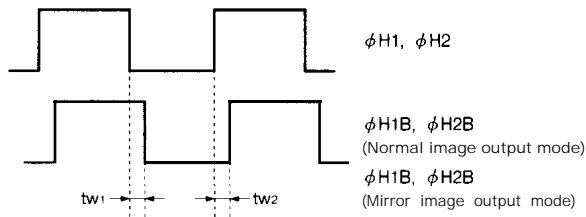
| PARAMETER | SYMBOL | RATING | UNIT |
|--|------------------------------|-------------|------|
| Output transistor drain voltage | V _{OD} | 0 to +18 | V |
| Reset transistor drain voltage | V _{RD} | 0 to +18 | V |
| Overflow drain voltage | V _{OFD} | 0 to +55 | V |
| Reset gate clock voltage | V ϕ_{RS} | -0.3 to +18 | V |
| Vertical shift register clock voltage | V ϕ_V | -9.0 to +18 | V |
| Horizontal shift register clock voltage | V ϕ_H | -0.3 to +18 | V |
| Voltage difference between PW and vertical clock | V _{PW} - V ϕ_V | -27 to 0 | V |
| Storage temperature | T _{stg} | -40 to +85 | °C |
| Operating ambient temperature | T _{opr} | -20 to +70 | °C |

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | SYMBOL | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|------------------------------------|------------------------------------|--------------|----------|---------------|------|------|
| Operating ambient temperature | | T_{op1} | | 25.0 | | °C | |
| Output transistor drain voltage | | V_{OD} | 14.5 | 15.0 | 16.0 | v | |
| Reset transistor drain voltage | | V_{RD} | | V_{OD} | | v | |
| Overflow drain voltage | When DC is applied | V_{Om} | 5.0 | | 19.0 | v | 1 |
| | When pulse is applied p-p level | $V_{\phi OFD}$ | 22.0 | | | v | 2 |
| Analog part ground voltage | | AGND | | 0.0 | | v | |
| Clock part ground voltage | | CGND | | 0.0 | | v | |
| P-well voltage | | VPW | -9.0 | | $V_{\phi VL}$ | V | |
| Vertical shift register clock | LOW level | $V_{\phi V1-4L}$ | -8.5 | -8.0 | -7.5 | v | |
| | INTERMEDIATE level | $V_{\phi V1-4I}$ | | 0.0 | | v | |
| | HIGH level | $V_{\phi V1H}, V_{\phi V3H}$ | 16.0 | 16.5 | 17.0 | v | |
| Horizontal shift register clock | LOW level | $V_{\phi H1-2L}, V_{\phi H1B-2BL}$ | -0.05 | 0.0 | 0.05 | V | |
| | HIGH level | $V_{\phi H1-2H}, V_{\phi H1B-2BH}$ | 4.7 | 5.0 | 6.0 | V | |
| Reset gate clock | LOW level | $V_{\phi RSL}$ | 0.0 | | $V_{RD}-12.0$ | v | |
| | HIGH level | $V_{\phi RSH}$ | $V_{RD}-7.5$ | | 9.5 | v | |
| Vertical shift register clock frequency | | $f_{\phi V1-4}$ | | 15.63 | | kHz | |
| Horizontal shift register clock frequency | | $f_{\phi H1-2}, f_{\phi H1B-2B}$ | | 9.66 | | MHz | |
| Reset gate clock frequency | | $f_{\phi RS}$ | | 9.66 | | MHz | |
| Horizontal shift register clock phase | | $tw1, tw2$ | 0.0 | 5.0 | 10.0 | ns | 3 |

NOTES :

1. When DC voltage is applied, shutter speed is 1 / 50 seconds,
2. When pulse is applied, shutter speed is less than 1 / 50 seconds
- 3.



ELECTRICAL CHARACTERISTICS (Drive method: Field Accumulation)

(Ta = 25°C, Operating conditions : typical values for the recommended operating conditions, Color temperature of light source : 3200 K / IR cut-off filter (CM-500, 1 mmt))

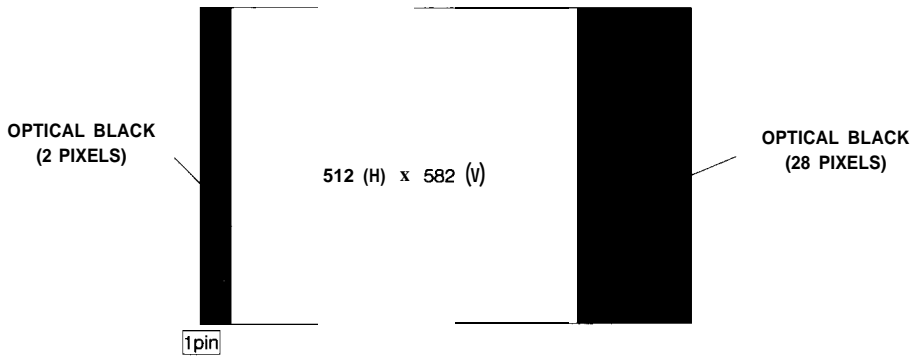
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | NOTE |
|---------------------------------|-----------------|------|-------|-------|------|------|
| Photo response non-uniformity | PRNU | | | 10 | % | 2 |
| Saturation signal | Vsat | 450 | | | mV | 3 |
| Dark output voltage | Vdark | | 0.3 | 3.0 | mV | 1, 4 |
| Dark signal non-uniformity | DSNU | | 0.6 | 2.0 | mV | 1, 5 |
| Sensitivity | R | 360 | 500 | | mV | 6 |
| Gamma | Y | | 1 | | | |
| Smear ratio | SMR | | 0.009 | 0.016 | % | 7 |
| Image lag | AI | | | 1.0 | % | 8 |
| Blooming suppression ratio | ABL | 1000 | | | | 9 |
| Output transistor drain current | I _{oD} | | 4.0 | 8.0 | mA | |
| Output impedance | R _o | | 300 | | Ω | |
| Dark noise | Vnoise | | 0.2 | 0.4 | mV | 10 |
| OB difference in level | | | | 1.0 | mV | 11 |

- The standard output voltage is defined as 150 mV by the average output voltage under uniform illumination.
- The standard exposure level is defined when the average output voltage is 150 mV under uniform illumination.

NOTES :

1. Ta : +60°C
2. The image area is divided into 10X 10 segments. The segment's voltage is the average output voltage of all the pixels within the segment. PRNU is defined by $(V_{max} - V_{min})/V_o$, where V_{max} and V_{min} are the maximum and the minimum values of each segment's voltage respectively, when the average output voltage V_o is 150 mV.
3. The image area is divided into 10x 10 segments.
The saturation signal is defined as the minimum of each segment's voltage which is the average output voltage of all the pixels within the segment, when the exposure level is set as 10 times, compared to standard level.
4. The average output voltage under a non-exposure condition.
5. The image area is divided into 10X 10 segments. DSNU is defined by $(V_{dmax} - V_{dmin})$ under the non-exposure condition where V_{dmax} and V_{dmin} are the maximum and the minimum values of each segment's voltage, respectively, that is the average output voltage over all pixels in the segment.
6. The average output voltage when a 1000 lux light source attached with a 90% reflector is imaged by a lens of F4, f50 mm.
7. The sensor is adjusted to position a V/I O square at the center of image area where V is the vertical length of the image area. SMR is defined by the ratio of the output voltage detected during the vertical blanking period to the maximum of the pixel voltage in the V/I O square.
8. The sensor is exposed at the exposure level corresponding to the standard condition preceding non-exposure condition. AI is defined by the ratio between the output voltage measured at the 1st field during the non-exposure period and the standard output voltage.
9. The sensor is adjusted to position a V/I O square at the center of image area. ABL is the ratio between the exposure at the standard condition and the exposure at a point where a blooming is observed.
10. The RMS value of the dark noise (after CDS). The bandwidth range is from 100 kHz to 5.0 MHz.
11. The difference between the average output voltage of the effective area and the OB part under the non-exposure condition.

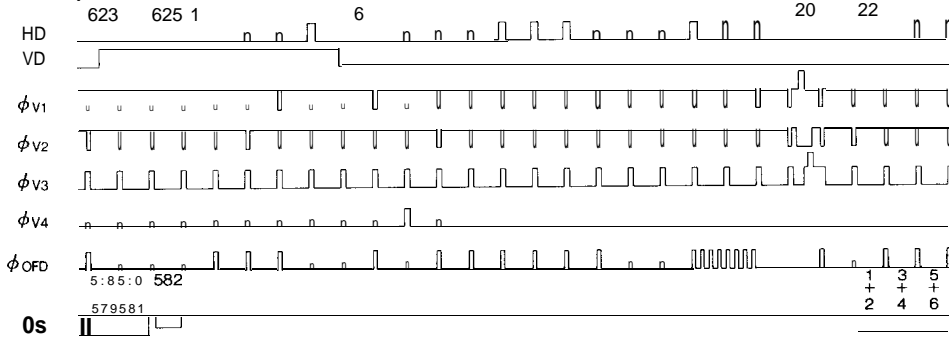
PIXEL STRUCTURE



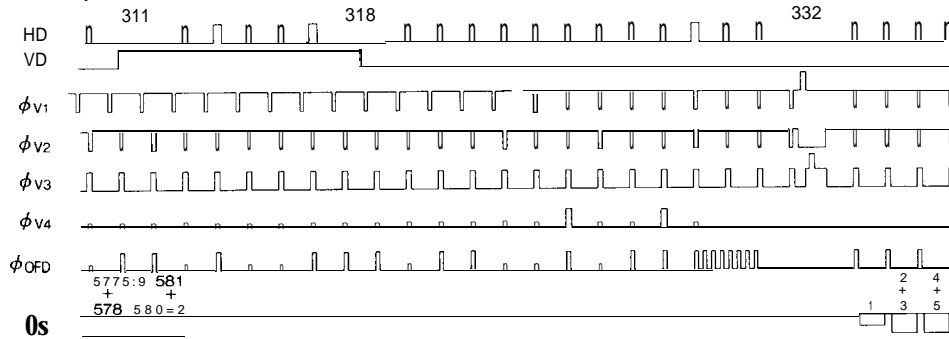
TIMING DIAGRAM EXAMPLE

VERTICAL TRANSFER TIMING < NORMAL OUTPUT > Shutter speed 1/10000 s

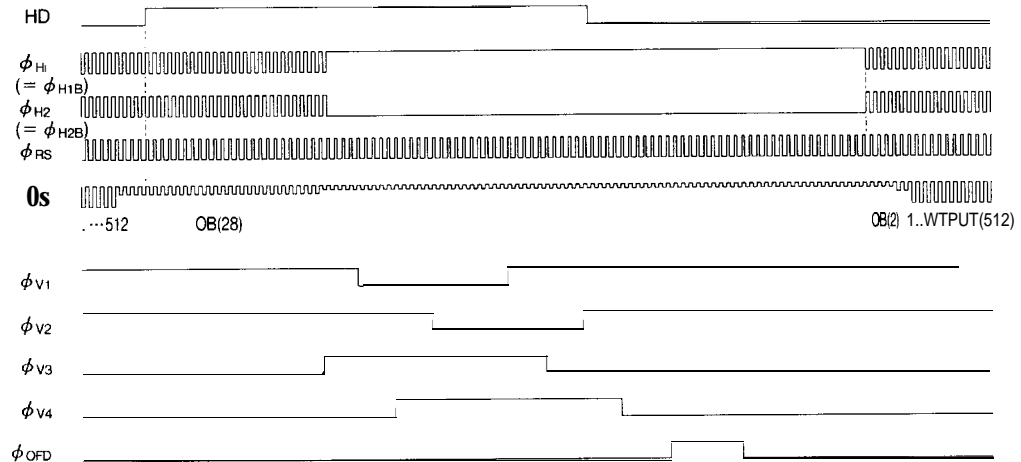
(1st, 3rd FIELD)



(2nd, 4th FIELD)



HORIZONTAL TRANSFER TIMING < NORMAL OUTPUT >

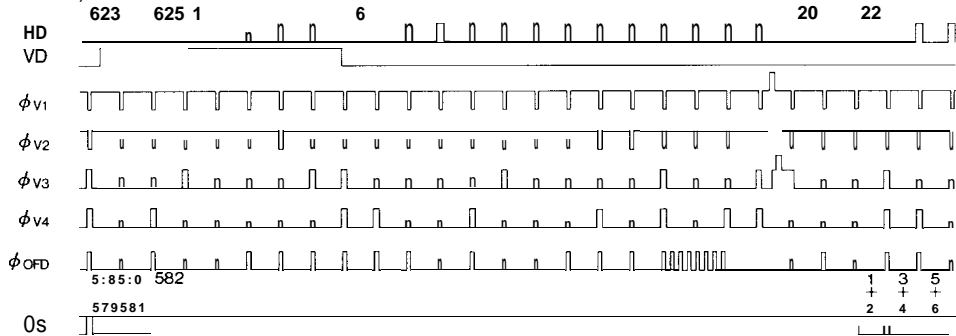


CCD AREA SENSORS
2

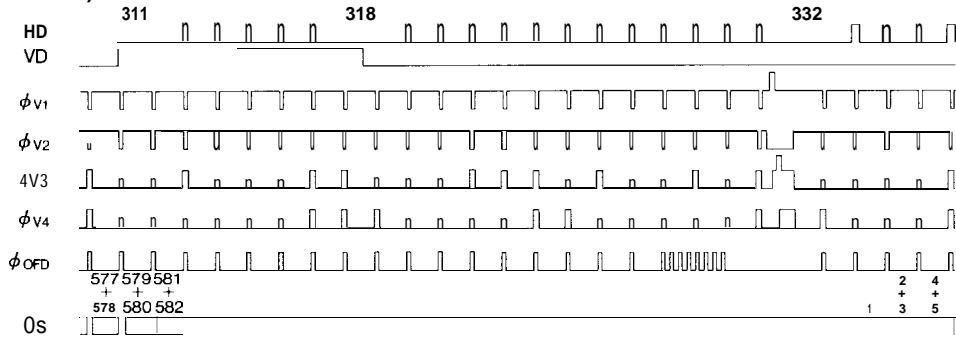
VERTICAL TRANSFER TIMING < MIRROR OUTPUT > Shutter speed

1/10000 s

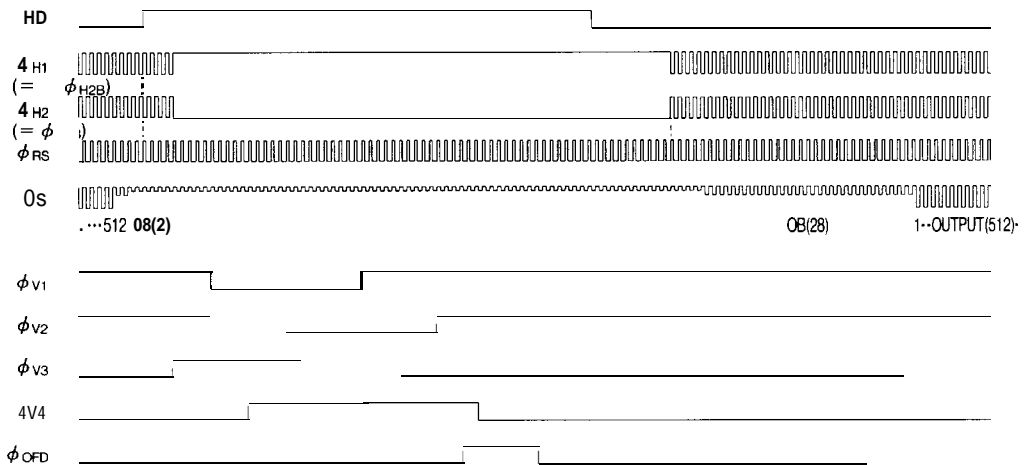
(1st, 3rd FIELD)



(2nd, 4th FIELD)



HORIZONTAL TRANSFER TIMING < MIRROR OUTPUT >



SYSTEM CONFIGURATION EXAMPLE

